**What is claimed is:**

1. A method of controlling the top width of a deep trench, comprising the steps of:

providing a substrate having a trench therein;

forming a first conductive layer and filling a portion of the trench;

forming a α-silicon layer on the sidewall of the trench and the first conductive layer, wherein the α-silicon is thicker at the top of the trench than elsewhere;

oxidizing the α-silicon layer to form a silicon oxide layer;

forming a dielectric layer on the silicon oxide layer, and anisotropically etching the dielectric layer and the silicon oxide layer to form a collar dielectric layer on the sidewalls of the trench;

forming a second conductive layer to fill the trench, with a lower surface than the trench; and

recessing the collar dielectric layer below the second conductive layer such that the substrate surface at the sidewall of the trench is exposed.

2. The method of controlling the top width of a deep trench as claimed in claim 1, wherein the substrate is a single crystal silicon substrate.

3. The method of controlling the top width of a deep trench as claimed in claim 1, formation of the first conductive layer further comprising:

depositing the conductive layer on the substrate and filling into the trench; and

etching back the conductive layer to form a recess in the trench.

4. The method of controlling the top width of a deep trench as claimed in claim 3, wherein the conductive layer is formed by chemical vapor deposition.

5. The method of controlling the top width of a deep trench as claimed in claim 3, wherein the conductive layer is etched by anisotropic dry etching.

6. The method of controlling the top width of a deep trench as claimed in claim 1, wherein the first conductive layer is an $n^+$-type doped polysilicon.

7. The method of controlling the top width of a deep trench as claimed in claim 1, the trench further comprising a capacitor and the conductive layer acting as a top electrode of the capacitor.

8. The method of controlling the top width of a deep trench as claimed in claim 1, wherein the α-silicon is thicker at the top than the bottom.

9. The method of controlling the top width of a deep trench as claimed in claim 8, wherein the thicker α-silicon at the top of the trench is formed by chemical vapor deposition.

10. The method of controlling the top width of a deep trench as claimed in claim 1, the steps of forming the second conductive layer further comprising:

depositing the conductive layer on the substrate and filling into the trench; and

etching back the conductive layer to form a recess in the trench.

11. The method of controlling the top width of a deep trench as claimed in claim 1, wherein the dielectric layer is TEOS oxide.

12. The method of controlling the top width of a deep trench as claimed in claim 1, wherein a portion of the silicon oxide and the collar dielectric is removed by wet etching.

13. A method of controlling the top width of a deep trench, comprising the steps of:

providing a semiconductor silicon substrate having a trench therein, and filling a first polysilicon layer in a portion of the trench;

forming a α-silicon layer on the sidewall of the trench and the first conductive layer, with α-silicon at the top of the trench being thicker than elsewhere;

oxidizing the α-silicon layer to form a silicon oxide layer;

forming a dielectric layer on the silicon oxide layer, and anisotropically etching the dielectric and

silicon oxide layer to form a collar dielectric layer on the sidewall of the trench;

forming a second conductive layer and filling into the trench, having a lower surface than the trench, and;

removing a portion of the collar dielectric layer, forming a surface lower than the second conductive layer.

14. The method of controlling the top width of a deep trench as claimed in claim 13, wherein the substrate is a single crystal silicon substrate.

15. The method of controlling the top width of a deep trench as claimed in claim 13, formation of the first conductive layer further comprising:

depositing the conductive layer on the substrate and filling the trench; and

etching back the conductive layer to form a recess in the trench.

16. The method of controlling the top width of a deep trench as claimed in claim 15, wherein the first conductive layer is formed by chemical vapor deposition.

17. The method of controlling the top width of a deep trench as claimed in claim 13, wherein the first conductive layer is etched by anisotropic dry etching.

18. The method of controlling the top width of a deep trench as claimed in claim 13, wherein the first conductive layer is an $n^+$-type doped polysilicon.

19. The method of controlling the top width of a deep trench as claimed in claim 13, the trench further comprising a capacitor and the conductive layer acting as a top electrode of the capacitor.

20. The method of controlling the top width of a deep trench as claimed in claim 13, wherein the α-silicon is thicker at the top than the bottom.

21. The method of controlling the top width of a deep trench as claimed in claim 20, wherein the thicker α-silicon is formed by chemical vapor deposition.

22. The method of controlling the top width of a deep trench as claimed in claim 13, the steps of forming the second conductive layer further comprising:

depositing the conductive layer on the substrate and filling into the trench; and

etching the conductive layer to form a recess in the trench.

23. The method of controlling the top width of a deep trench as claimed in claim 13, wherein the dielectric layer is TEOS oxide.

24. The method of controlling the top width of a deep trench as claimed in claim 13, wherein a portion of the silicon oxide and the collar dielectric is removed by wet etching.